

IN THE CLAIMS

1. (currently amended) An integrated circuit device adapted to be loaded in host equipment, comprising:

a substantially rectangular main body unit;

a first set of connection terminals provided at one end of said main body unit to enable electrical connection between said main body unit and the host equipment;

a plurality of loading sections provided in said main body unit, each of said loading sections having an insertion opening along an edge of said main body unit transverse to said one end, a second set of connection terminals spaced from said insertion opening, and a pair of sidewalls disposed between said insertion opening and said second set of connection terminals;

a plurality of substantially rectangular integrated circuit chips assembled in respective ones of said loading sections, each of said integrated circuit chips including a built-in integrated circuit unit forming a memory unit or a logic circuit and a third set of connection terminals for establishing electrical connection between said second set of connection terminals in said loading section and said integrated circuit unit;

a guide support provided in each of said loading sections and extending in a direction transverse to said insertion opening for guiding the insertion of said integrated circuit chips into said loading section, each said guide support including a pair of guide recesses formed along said pair of sidewalls of said loading section; and

a controller disposed in said main body unit for controlling the writing of information signals to and the readout of information signals from said plurality of integrated circuit chips loaded in said loading sections, said controller including:

a memory controller for concurrently controlling data writing and reading to each of said integrated circuit chips assembled in said respective ones of said loading sections;

an interface for enabling data exchange between said controller and the host equipment;

a register logically associated with said memory controller and said interface and having a variety of parameters for data exchange; and

a buffer logically associated with said memory controller and said interface for transient data storage.

2. (currently amended) A memory device adapted to be loaded in host equipment, comprising:

a substantially rectangular main body unit;

a first set of connection terminals provided at one end of said main body unit to enable electrical connection between said main body unit and the host equipment;

a plurality of loading sections provided in said main body unit, each of said loading sections having an insertion opening along an edge of said main body unit transverse to said one end, a second set of connection terminals spaced from said insertion opening, and a pair of sidewalls disposed between said insertion opening and said second set of connection terminals;

a plurality of substantially rectangular memory chips assembled in respective ones of said loading sections, each of said memory chips including a memory unit therein and a third set of connection terminals for establishing electrical connection between said second set of connection terminals in said loading section and said memory unit;

a guide support provided in each of said loading sections and extending in a direction transverse to said insertion opening for guiding the insertion of said memory chips

into said loading section, each said guide support including a pair of guide recesses formed along said pair of sidewalls of said loading section; and

a controller disposed in said main body unit for controlling the writing of information signals to and the readout of information signals from said plurality of memory chips loaded in said loading sections, said controller including:

a memory controller for concurrently controlling data writing and reading to each of said integrated circuit chips assembled in said respective ones of said loading sections;

an interface for enabling data exchange between said controller and the host equipment;

a register logically associated with said memory controller and said interface and having a variety of parameters for data exchange; and

a buffer logically associated with said memory controller and said interface for transient data storage.

3. (previously presented) The memory device according to claim 2, wherein said main body unit has a width of approximately 21.45 mm, a length of approximately 50 mm and a thickness of approximately 2.8 mm.

4. (original) The memory device according to claim 2, wherein said memory unit is a flash memory.

5. (currently amended) An adapter device adapted to be loaded in host equipment, comprising:

a substantially rectangular main body unit;

a first set of connection terminals provided at one end of said main body unit to enable electrical connection between said main body unit and the host equipment;

a plurality of loading sections provided in said main body unit, each of said loading sections having an insertion opening along an edge of said main body unit transverse to said one end, a second set of connection terminals spaced from said insertion opening, and a pair of sidewalls disposed between said insertion opening and said second set of connection terminals;

a plurality of substantially rectangular integrated circuit chips or dummy chips assembled in respective ones of said loading sections, each of said integrated circuit chips including a built-in integrated circuit unit forming a memory unit or a logic circuit in electrical connection with said second set of connection terminals in said loading section, each of said dummy chips being of substantially the same shape as said integrated circuit chips;

a guide support provided in each of said loading sections and extending in a direction transverse to said insertion opening for guiding the insertion of said integrated circuit chips or said dummy chips into said loading section, each said guide support including a pair of guide recesses formed along said pair of sidewalls of said loading section; and

a controller disposed in said main body unit for controlling said integrated circuit chips loaded in said loading sections, said controller including:

a memory controller for concurrently controlling data writing and reading to each of said integrated circuit chips assembled in said respective ones of said loading sections;

an interface for enabling data exchange between said controller and the host equipment;

a register logically associated with said memory controller and said interface and having a variety of parameters for data exchange; and

a buffer logically associated with said memory controller and said interface for transient data storage.

6. (currently amended) A substantially rectangular integrated circuit chip adapted to be loaded in an adaptor device for use in host equipment, said integrated circuit chip comprising:

a main body unit removably insertable into the adaptor device and having a pair of sidewalls;

an integrated circuit unit disposed in said main body unit, said integrated circuit unit comprising a copyright protection circuit unit;

a set of terminals provided at one end of said main body unit for establishing an electrical connection enabling information signals to be exchanged between said integrated circuit unit and the adaptor device; and

a guide support unit including a pair of protuberantly formed guide sections provided on said pair of sidewalls of said main body unit for guiding the insertion of said main body unit into a pair of guide recesses disposed along sidewalls of the adaptor device;

wherein, when said integrated circuit chip is loaded in the adaptor device along with a separate memory device, said copyright protection circuit unit is operable to authenticate the separate memory device to protect copyrighted data stored on the separate memory device.

7-9. (canceled)

10. (new) The integrated circuit chip of claim 6, wherein said copyright protection circuit unit includes a built-in logic circuit for authenticating a user ID of the separate memory device.

11. (new) The integrated circuit device of claim 1, wherein said logic circuit of one of said integrated circuit chips comprises a copyright protection circuit unit that is operable to authenticate said memory unit of another one of said integrated circuit chips to protect copyrighted data stored on said memory unit of said another integrated circuit chip.

12. (new) The integrated circuit device of claim 11, wherein said copyright protection circuit unit authenticates a user ID associated with said memory unit of said another integrated circuit chip.

13. (new) The memory device of claim 2, further comprising a copyright protection circuit chip assembled in one of said loading sections that is operable to authenticate said memory unit of at least one of said memory chips to protect copyrighted data stored therein.

14. (new) The memory device of claim 13, wherein said copyright protection circuit chip authenticates said memory unit based on a user ID associated with said memory unit.

15. (new) The adapter device of claim 5, wherein said logic circuit of one of said integrated circuit chips comprises a copyright protection circuit unit that is operable to authenticate said memory unit of another one of said integrated circuit chips to protect copyrighted data stored on said memory unit of said another integrated circuit chip.

16. (new) The adapter device of claim 15, wherein said copyright protection circuit unit authenticates a user ID associated with said memory unit of said another integrated circuit chip.